

Fig. 1 IGBT with Monolithic or Discrete Diode Collector to Gate Clamp Circuit

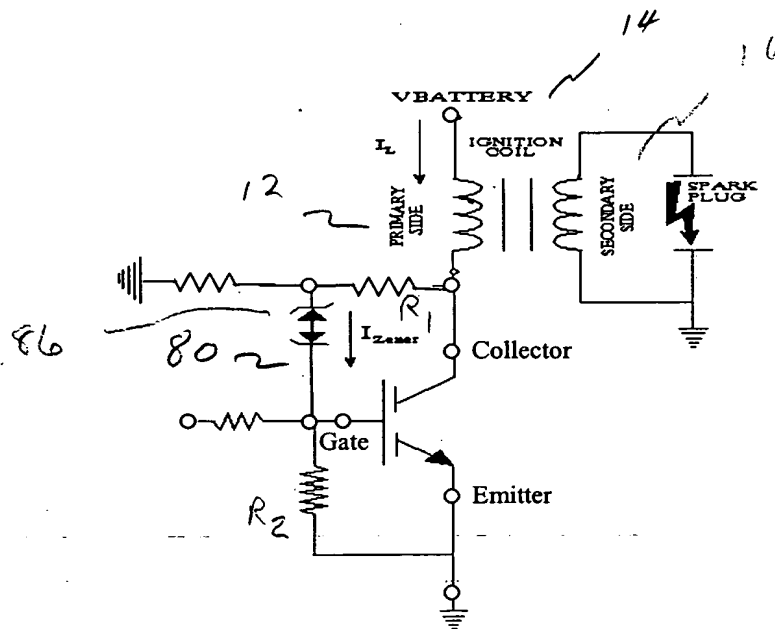


Fig. 2 IGBT with Monolithic or Discrete Resistive Voltage Divider and Diode Collector to Gate Clamp Circuit

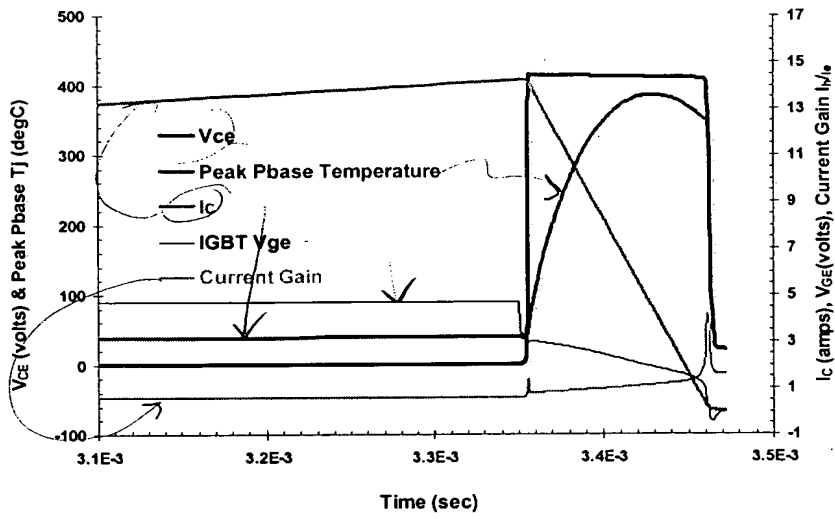


Fig. 3 Simulated 14.2A, 310mJ SCIS stress for and IGBT used in the circuit of Fig 1.

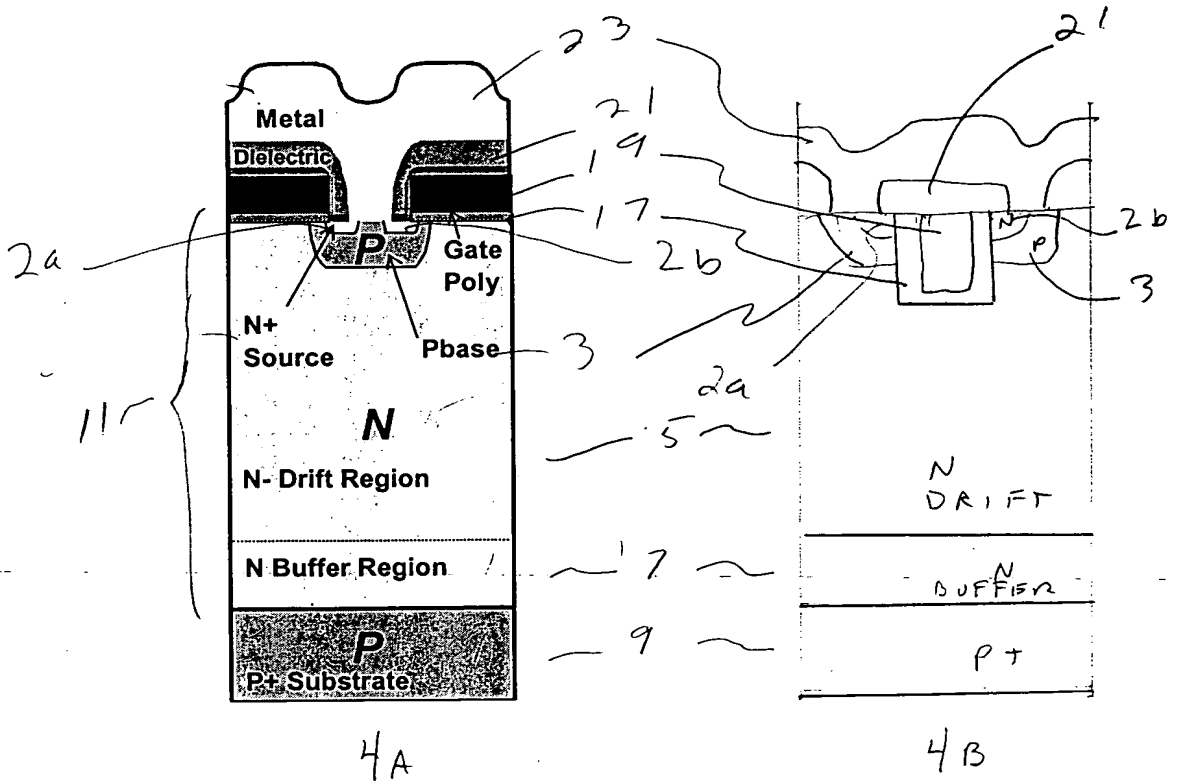
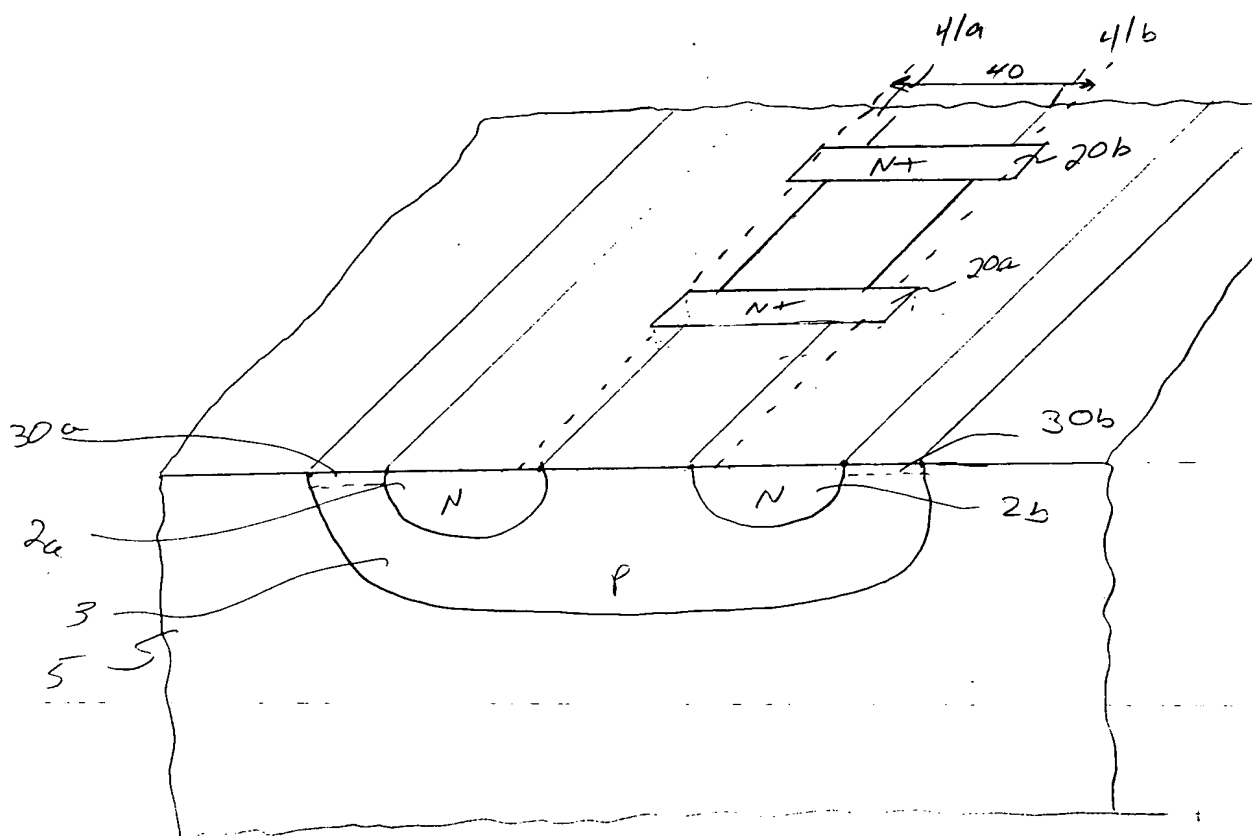


Fig. 4 Typical IGBT stripe cell vertical cross-section .

This diagram shows a cross-sectional view of a semiconductor device. It features a substrate with a central region labeled 'P' and two side regions labeled 'N'. Two gates, labeled '2a' and '2b', are positioned on top of the 'N' regions. Each gate contains a rectangular opening, labeled '19a' and '19b' respectively. The gates are connected to a common line labeled '40'. The device is surrounded by a layer labeled '3', and the entire structure is enclosed in a layer labeled '5'. The regions are labeled '2a', '2b', '3', '4a', '4b', '4c', '4d', '4e', '4f', '4g', '4h', '4i', '4j', '4k', '4l', '4m', '4n', '4o', '4p', '4q', '4r', '4s', '4t', '4u', '4v', '4w', '4x', '4y', '4z', '4aa', '4ab', '4ac', '4ad', '4ae', '4af', '4ag', '4ah', '4ai', '4aj', '4ak', '4al', '4am', '4an', '4ao', '4ap', '4aq', '4ar', '4as', '4at', '4au', '4av', '4aw', '4ax', '4ay', '4az', '4ba', '4bb', '4bc', '4bd', '4be', '4bf', '4bg', '4bh', '4bi', '4bj', '4bk', '4bl', '4bm', '4bn', '4bo', '4bp', '4bq', '4br', '4bs', '4bt', '4bu', '4bv', '4bw', '4bx', '4by', '4bz', '4ca', '4cb', '4cc', '4cd', '4ce', '4cf', '4cg', '4ch', '4ci', '4cj', '4ck', '4cl', '4cm', '4cn', '4co', '4cp', '4cq', '4cr', '4cs', '4ct', '4cu', '4cv', '4cw', '4cx', '4cy', '4cz', '4da', '4db', '4dc', '4dd', '4de', '4df', '4dg', '4dh', '4di', '4dj', '4dk', '4dl', '4dm', '4dn', '4do', '4dp', '4dq', '4dr', '4ds', '4dt', '4du', '4dv', '4dw', '4dx', '4dy', '4dz', '4ea', '4eb', '4ec', '4ed', '4ee', '4ef', '4eg', '4eh', '4ei', '4ej', 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This diagram shows a cross-sectional view of a semiconductor device. A central channel, labeled 40, is defined by a "Poly Opening" at the bottom. The channel is flanked by regions labeled 20a and 20b. Above the channel, there are regions labeled 41a and 41b. The device is surrounded by a "Pbase" region. At the bottom, there are "Poly" regions on either side of the "Poly Opening". The device is also labeled with "N Channel Doping" and "N JFET Region". Various other labels include 2a, 2b, 30a, 30b, 20c, 3b, 36, and 20a.

Fig. 5 Top view of stripe with full channel design . Contact to N Channel doping is along the entire length of the stripe.

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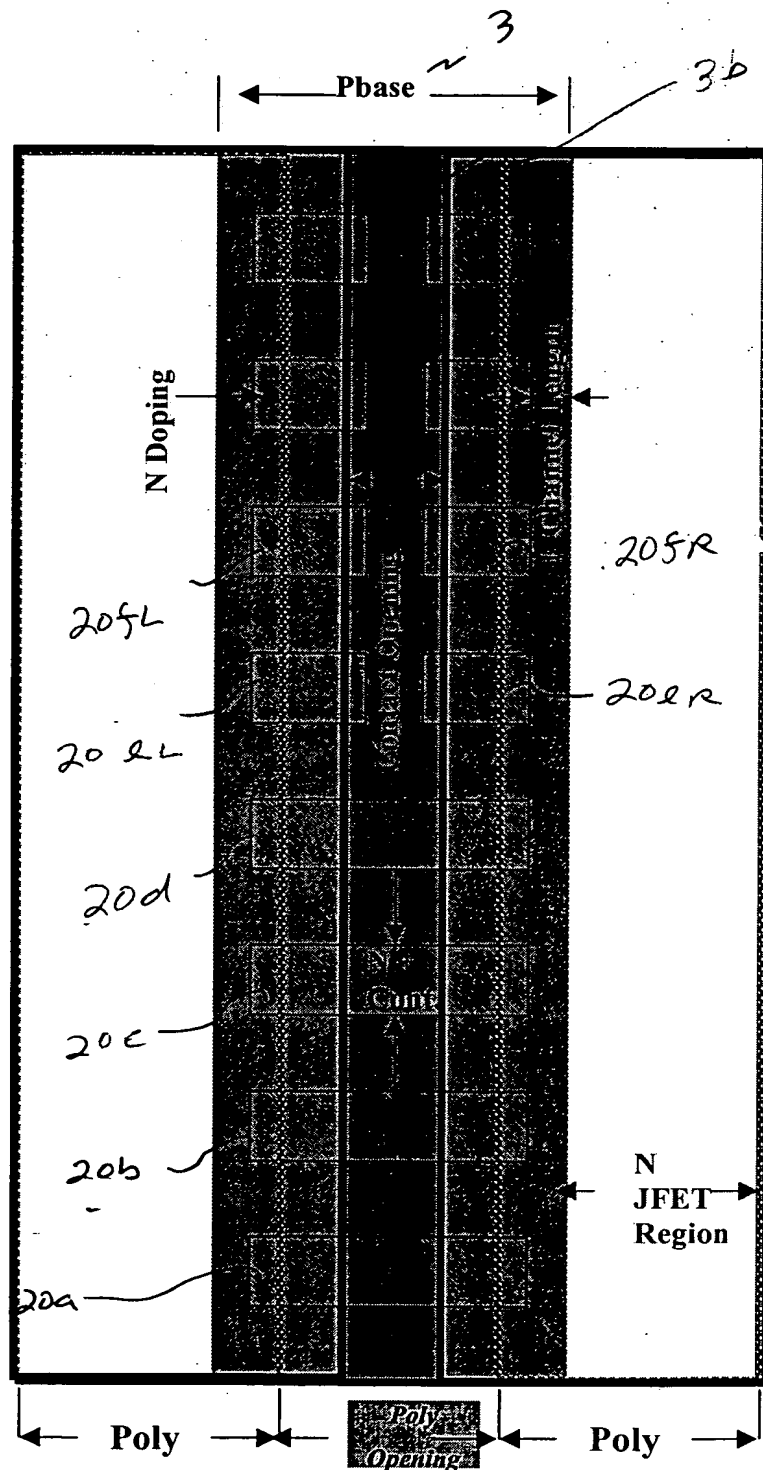


Fig. 6 Top view of stripe with channel version A exclude design. Top half of stripe separate N+ contacts. Bottom half of stripe continuous N+ contacts across the contact opening.

3

Phase

30

2a.3

T

30b

14

26.3

T

H

20b

2b.2

2a.2

T

30a

14

2a.1

N Doping

N JFET Region

11

2b.1

20a

Poly

Poly Opening

Poly

Fig. 7 Top view of stripe with Version B channel exclude design.

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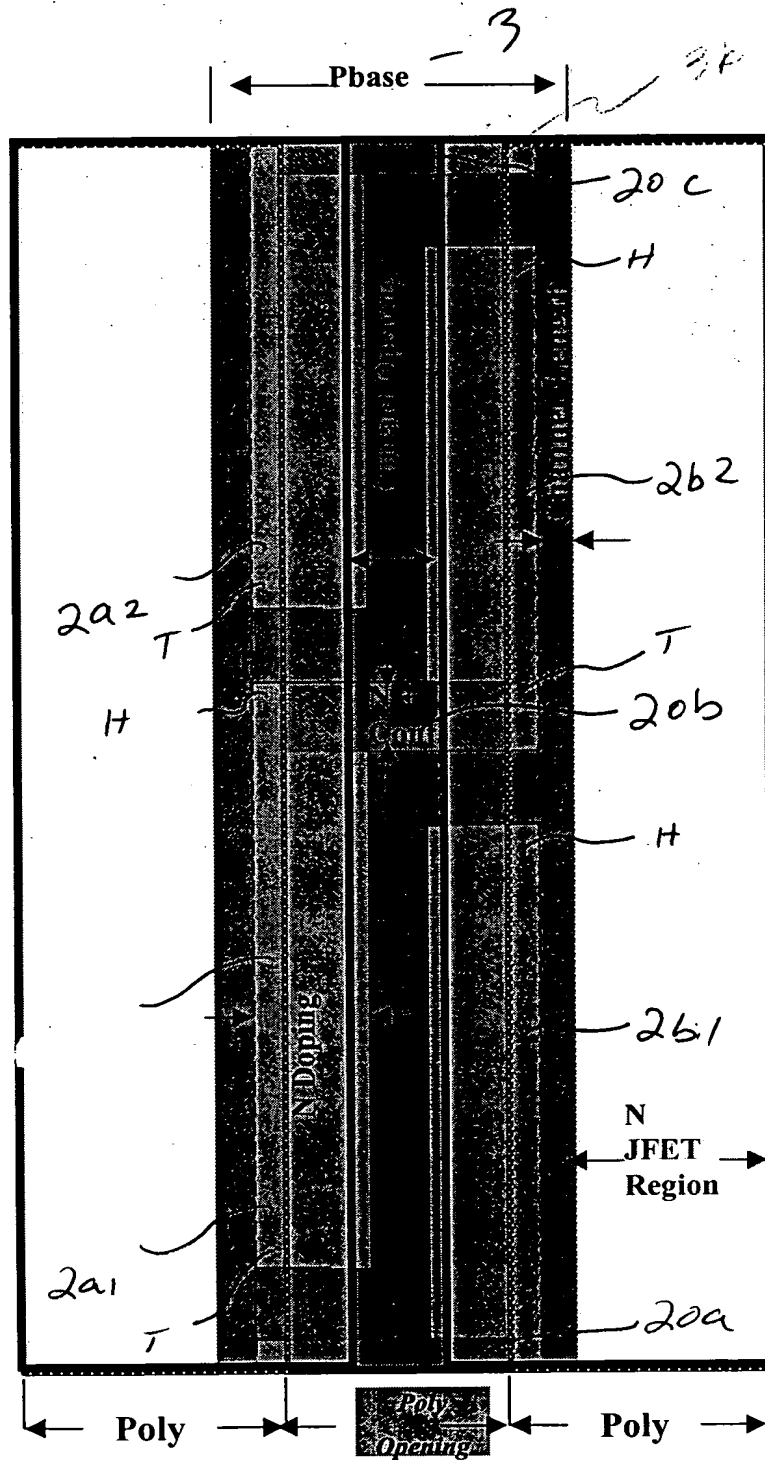


Fig. 8 Top view of stripe with Version C channel exclude design.

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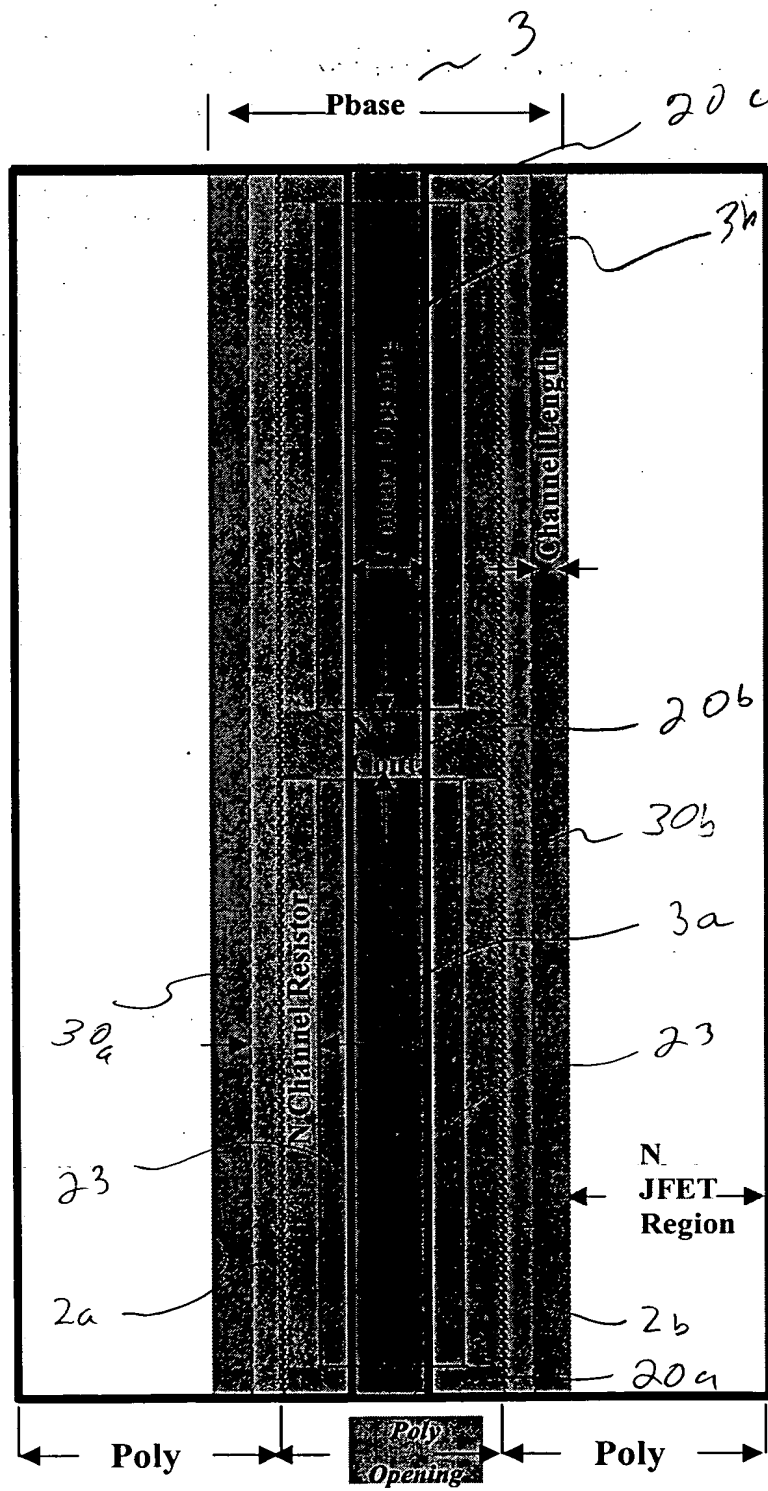


Fig. 9 Top view of stripe with full channel length channel resistor design.

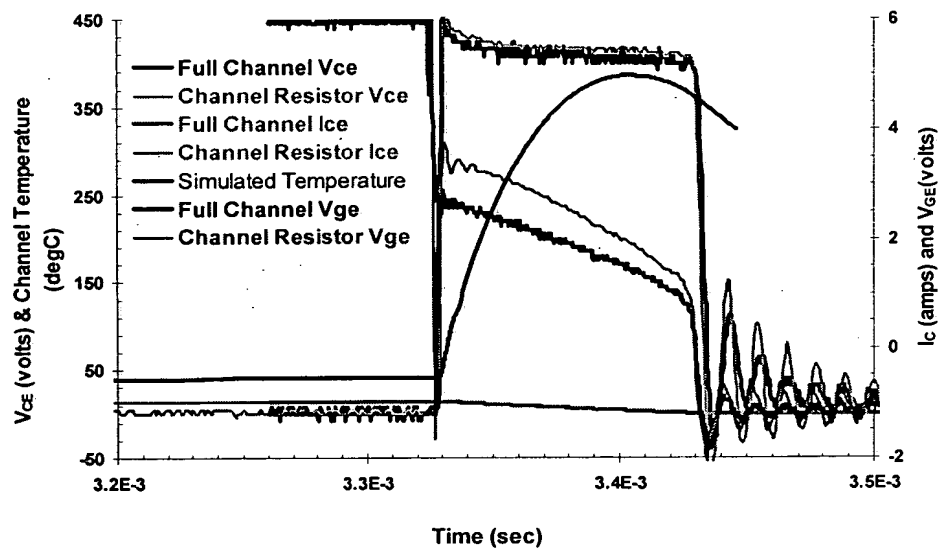


Fig. 10 Measured 27°C, 14.2A, $V_{ge}=5V$, $R_{ge}=1k\Omega$ SCIS Stress for full channel design in Fig 5 and invention shown in Fig 14 with channel resistor having equivalent active area.

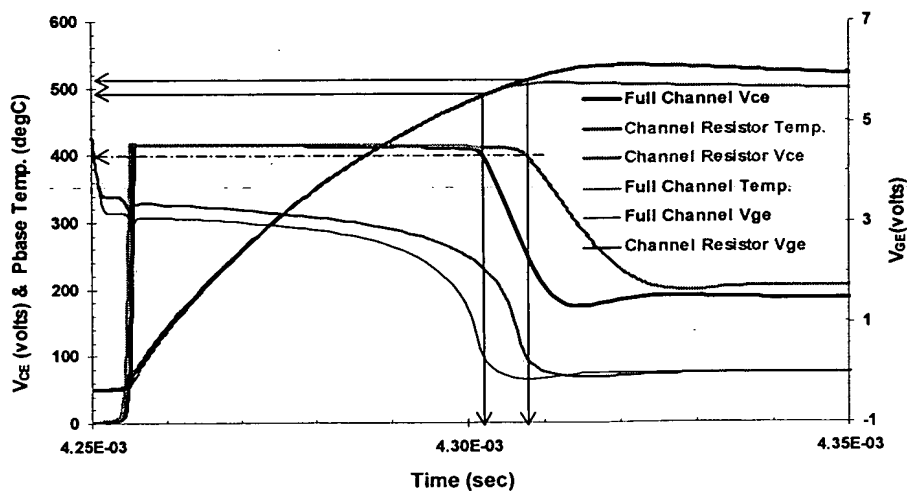


Fig. 11 Simulated 27°C, 17.8A, $V_{ge}=5V$, $R_{ge}=1k\Omega$ SCIS Stress for full channel design in Fig 5 and invention shown in Fig 14 with non-temperature compensated channel resistor having equivalent active area.

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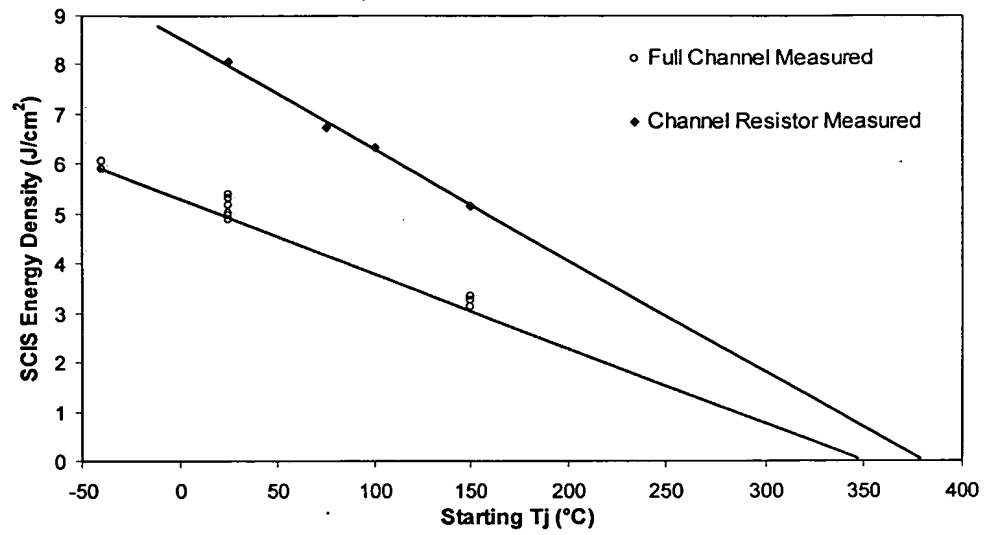


Fig. 12 Measured SCIS energy density capability with primary inductance of 3mH.

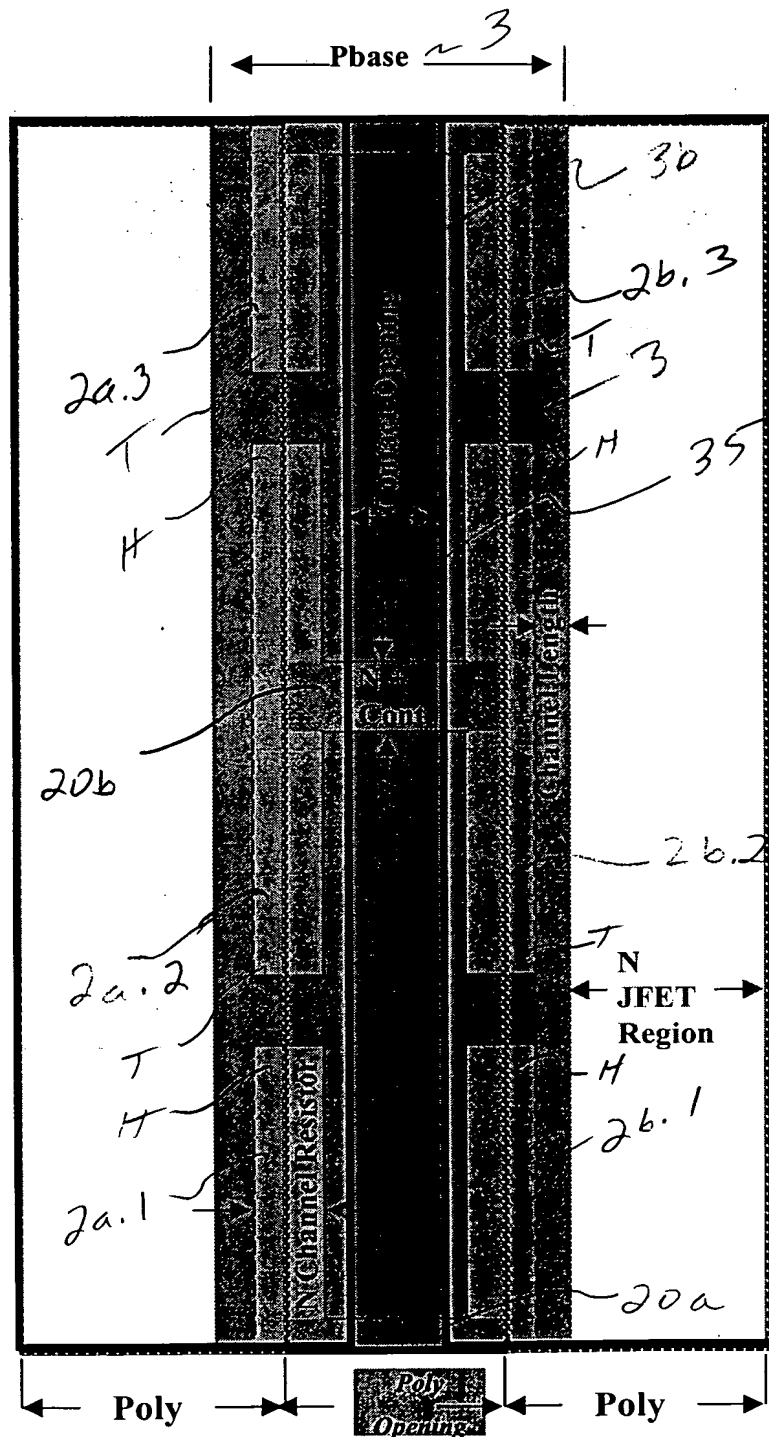


Fig. 13 Top view of stripe "H" pattern channel resistor design.

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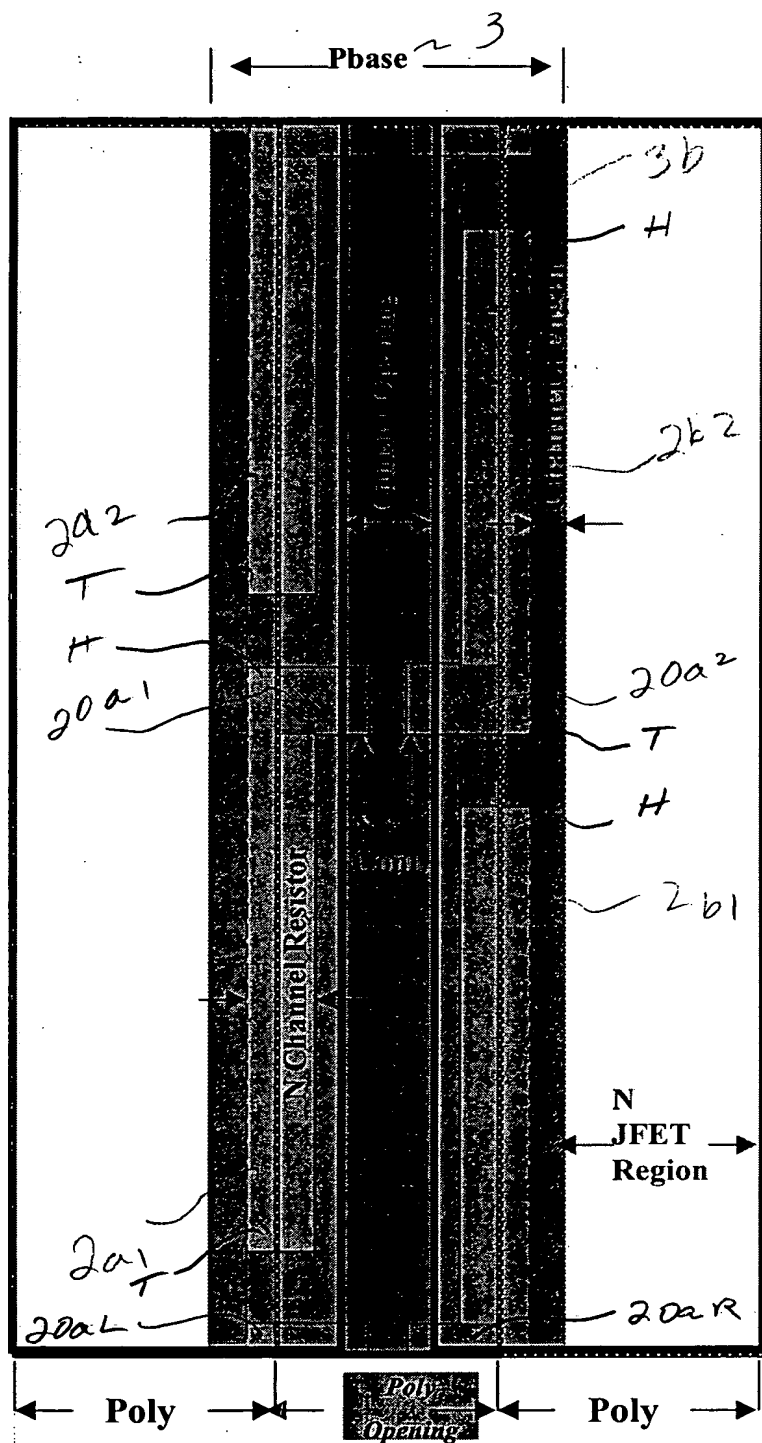


Fig. 14 Top view of stripe "H" pattern channel resistor design.

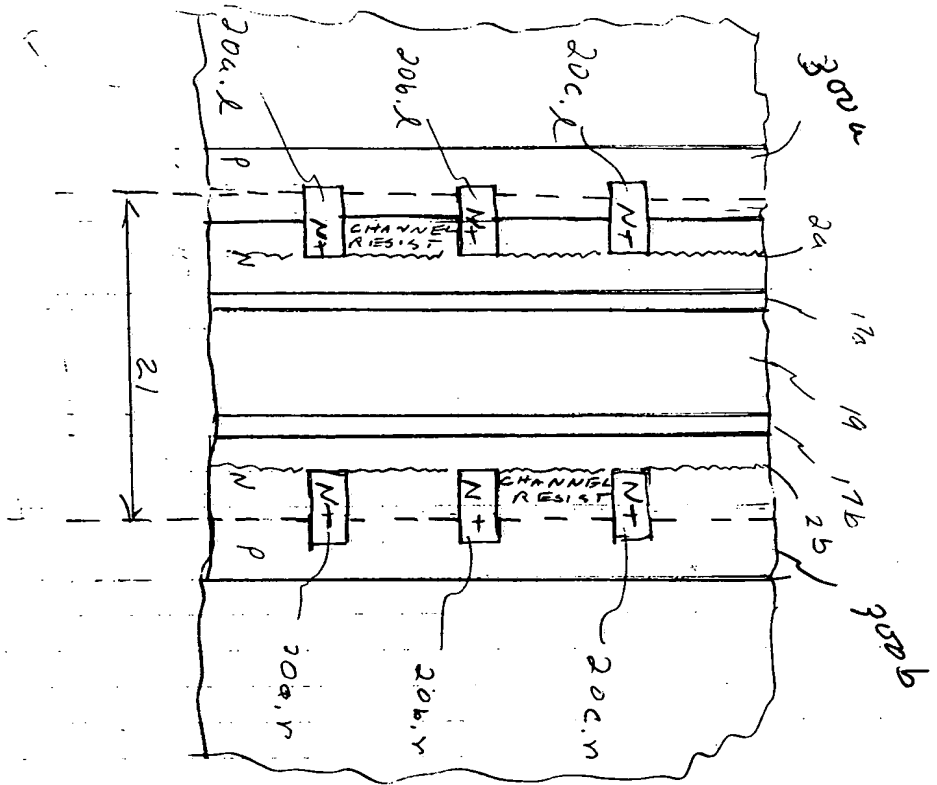


FIG. 15

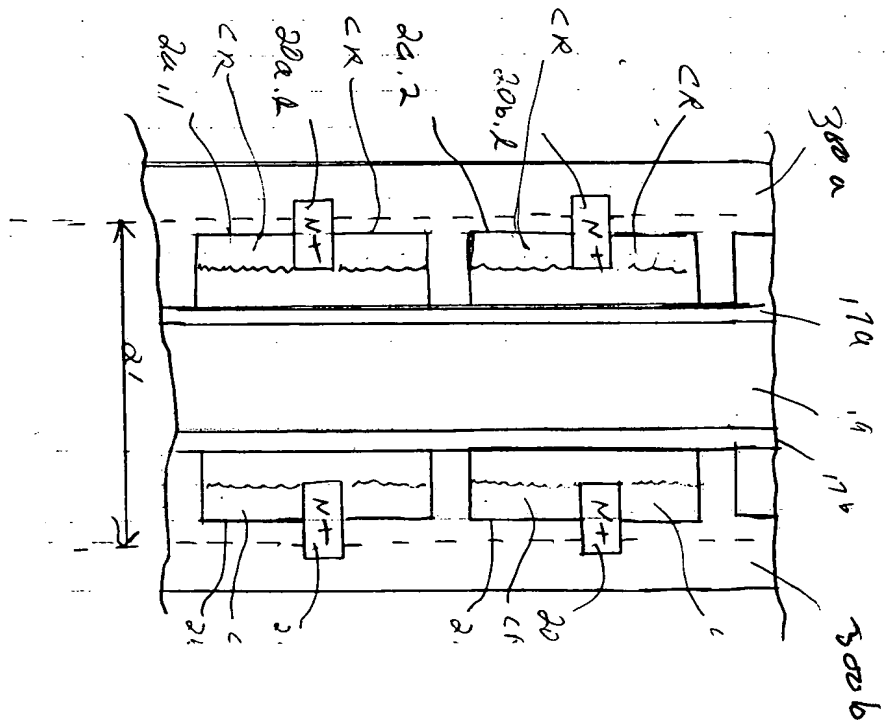


FIG. 16

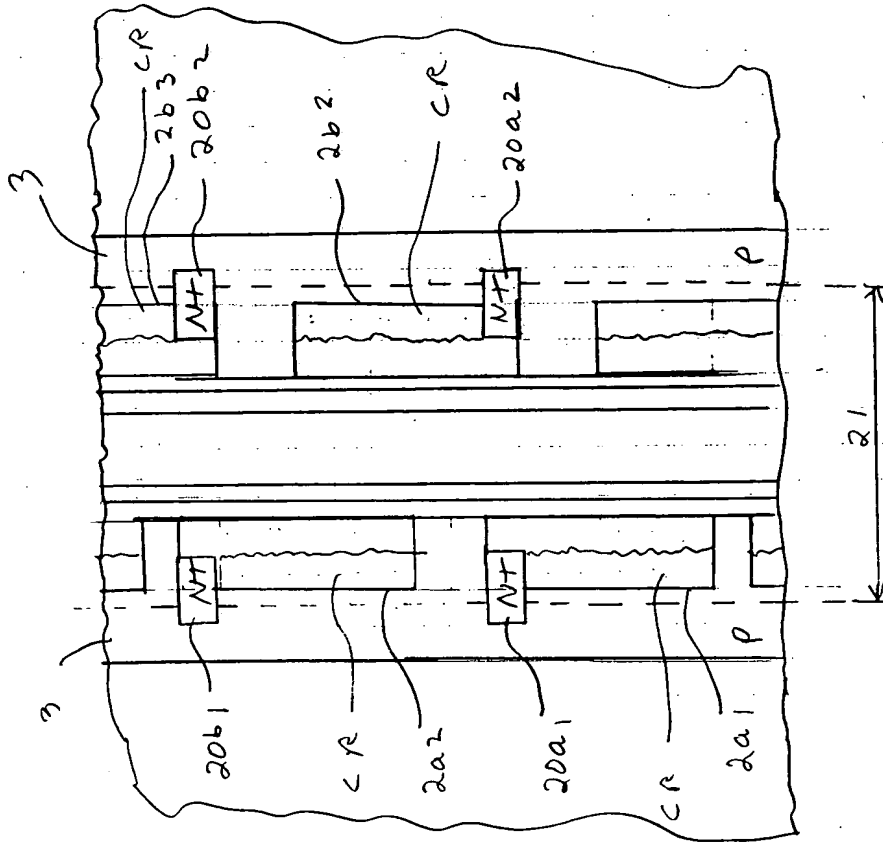


Fig. 17